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SCHWEGMAN LUNDBERG WOESSNER & KLUTH
P O BOX 2938
MINNEAPOLIS, MN 55402

EXAMINER	
PRENTY, MARK V	
ART UNIT	PAPER NUMBER
2822	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/132,157	FORBES, LEONARD	
	Examiner	Art Unit	
	MARK V PRENTY	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 October 2003 and 28 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *11,13,14,24-28,32 and 38-43* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *25 and 41-43* is/are allowed.

6)☒ Claim(s) *11, 13, 14, 24, 26-28 and 38-40* is/are rejected.

7)☒ Claim(s) *32* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

This Office Action is in response to the responses filed on October 14, 2003 and November 28, 2003.

As a preliminary matter, claim 25, line 2, contains a typographical error. Specifically, the "SiO_2" is a typographical error that should be deleted (see claim 25 as presented in the amendment filed November 28, 2001, which was the last time claim 25 was amended).

Claims 26 and 27 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Specifically, claims 26 and 27 are indefinite because "the Ge" lacks antecedent basis in independent claim 24, on which they depend. Claims 26 and 27 should apparently depend on independent claim 25, which recites Ge.

Claims 11, 24 and 38 are rejected under 35 U.S.C. §102(b) as being anticipated by Saito (newly cited Japanese Kokai 4-34942).

With respect to independent claim 11, Saito discloses a metal-oxide-semiconductor transistor[1] (see the entire Kokai, including the attached English language translation thereof), comprising: a silicon substrate 1; a silicon dioxide (SiO_2) gate oxide 3, coupled to the substrate; a gate 7, coupled to the SiO_2 gate oxide; source/drain regions 8/10 formed in the substrate on opposite sides of the gate; and a $Si_{1-x}Ge_x$ channel region 6, having a germanium molar fraction x, located underneath the SiO_2 gate oxide and between the source/drain regions (see the English translation at pages 4 and 5), wherein x is less than or equal to 0.6 (note that Saito's germanium ion implant

[1] Claim 11's "p-channel" preamble language is not given patentable weight. See *In re Hirao*, 535 F.2d 67, 190 USPQ 15 (CCPA 1976).

dosage is less than the applicant's disclosed germanium ion implant dosage), and wherein the $Si_{1-x}Ge_x$ channel region forms a continuous $Si_{1-x}Ge_x$ / SiO_2 gate oxide interface wherein no germanium oxide is present at the $Si_{1-x}Ge_x$ / SiO_2 gate oxide interface (as a result of ion implantation of germanium through the previously formed SiO_2 gate oxide).

Claim 11 is thus rejected under 35 U.S.C. §102(b) as being anticipated by Saito.

With respect to independent claim 24, Saito discloses a metal-oxide-semiconductor transistor[2] (see the entire Kokai, including the attached English language translation thereof), comprising: a $Si_{1-x}Ge_x$ channel region 6, having a germanium molar fraction of x, and formed in the substrate, underneath a silicon dioxide (SiO_2) gate oxide and between a source region and a drain region (see the English translation at pages 4 and 5); wherein x is less than or equal to 0.6 (note that Saito's germanium ion implant dosage is less than the applicant's disclosed germanium ion implant dosage), and wherein the $Si_{1-x}Ge_x$ channel region forms a continuous $Si_{1-x}Ge_x$ / SiO_2 gate oxide interface wherein no germanium oxide is present at the $Si_{1-x}Ge_x$ / SiO_2 gate oxide interface (as a result of ion implantation of germanium through the previously formed SiO_2 gate oxide).

Claim 24 is thus rejected under 35 U.S.C. §102(b) as being anticipated by Saito.

With respect to independent claim 38, Saito discloses a semiconductor transistor (see the entire Kokai, including the attached English language translation), comprising: a silicon substrate 1; a silicon dioxide (SiO_2) gate oxide 3, coupled to the substrate; a

[2] Claim 24's "p-channel" preamble language is not given patentable weight. See *In re Hirao*, 535 F.2d 67, 190 USPQ 15 (CCPA 1976).

gate 7, coupled to the SiO_2 gate oxide; source/drain regions 8/10 formed in the substrate on opposite sides of the gate; and a $Si_{1-x}Ge_x$ channel region 6, having a germanium molar fraction of x, located underneath the SiO_2 gate oxide and between the source/drain regions (see the English translation at pages 4 and 5), wherein x is less than or equal to 0.6 (note that Saito's germanium ion implant dosage is less than the applicant's disclosed germanium ion implant dosage), and wherein the $Si_{1-x}Ge_x$ channel region forms a continuous $Si_{1-x}Ge_x$ / SiO_2 gate oxide interface wherein no germanium oxide is present at the $Si_{1-x}Ge_x$ / SiO_2 gate oxide interface (as a result of ion implantation of germanium through the previously formed SiO_2 gate oxide).

Claim 38 is thus rejected under 35 U.S.C. §102(b) as being anticipated by Saito.

Claims 11, 13, 14, 24, 26-28 and 38-40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakagawa (United States Patent 5,272,365, already of record) together with Burghartz et al. (newly cited United States Patent 5,461,250 – hereafter Burghartz).

With respect to independent claim 11, Nakagawa discloses a p-channel metal-oxide-semiconductor transistor (see the entire patent, particularly the Fig. 3 disclosure), comprising: a silicon substrate 12; a silicon dioxide (SiO_2) gate oxide "34" (note that Fig. 3's "34" is essentially a typo that should be "18," as per the Figs. 1-2 disclosure, and see column 4, lines 27-28), coupled to the substrate; a gate 22, coupled to the SiO_2 gate oxide; source/drain regions 14 and 16 formed in the substrate on opposite sides of the gate; and a $Si_{1-x}Ge_x$ channel region 42, having a germanium molar fraction x, located underneath the SiO_2 gate oxide and between the source/drain regions, wherein x is less than or equal to 0.6 (see column 3, lines 21-25), and wherein the $Si_{1-x}Ge_x$

channel region 42 forms a continuous $Si_{1-x}Ge_x$ / SiO_2 gate oxide interface (with SiO_2 gate oxide "34").

Nakagawa discloses that the SiO_2 gate oxide 18 of at least its Fig. 1 and Fig. 2 embodiments is "thermal silicon oxide" (see column 2, lines 49-56, for example), which means that it is formed by thermally oxidizing an underlying silicon layer (Fig. 1's silicon layer 20 and Fig. 2's silicon layer 34).

Nakagawa's Fig. 3 gate oxide "34" (again, such should be "18," as per the Figs. 1-2 disclosure) is apparently similarly formed by thermally oxidizing Fig. 3's $Si_{1-x}Ge_x$ channel region 42 (see column 5, lines 19-35). Nakagawa does not disclose that germanium oxide is present at Fig. 3's $Si_{1-x}Ge_x$ / SiO_2 gate oxide interface, but the applicant maintains: "germanium oxide will necessarily be created at [Nakagawa's] $Si_{1-x}Ge_x$ / SiO_2 gate oxide interface" (applicant's October 14, 2003 response at page 8, first paragraph). The applicant's argument is accepted in order to advance prosecution.

The apparent difference between claim 11 and Nakagawa, therefore, is claim 11 recites: "no germanium oxide is present at the $Si_{1-x}Ge_x$ / SiO_2 gate oxide interface."

Burghartz teaches forming a SiO_2 gate oxide on a SiGe channel layer by depositing a SiO_2 gate oxide layer on the SiGe layer instead of by thermally oxidizing the SiGe layer (see the entire patent, particularly the Fig. 3 disclosure).

It would have been obvious to one skilled in this art to form Nakagawa's Fig. 3 SiO_2 gate oxide "34" (again, such should be "18") by depositing a SiO_2 gate oxide layer on SiGe region 42 instead of by thermal oxidizing SiGe region 42, as per Burghartz's teaching (and such would result in there being no germanium oxide present at the $Si_{1-x}Ge_x$ / SiO_2 gate oxide interface because the SiGe region is not oxidized).

Claim 11 is thus rejected under 35 U.S.C. 103(a) as being unpatentable over Nakagawa together with Burghartz.

With respect to dependent claim 13, although Nakagawa is silent as to the thickness of its $Si_{1-x}Ge_x$ channel region 42, Burghartz also teaches that a SiGe channel region is typically 10-50 nm (100-500 angstroms) thick (see column 7, lines 64-66).

It would have been further obvious to one skilled in this art to make Nakagawa's $Si_{1-x}Ge_x$ channel region 42 100-500 angstroms thick, because Burghartz teaches that $Si_{1-x}Ge_x$ channel regions are conventionally formed that thick.

Claim 13 is thus rejected under 35 U.S.C. 103(a) as being unpatentable over Nakagawa together with Burghartz.

With respect to dependent claim 14, Nakagawa's germanium molar fraction is approximately 0.2 (see column 3, lines 21-25).

Claim 14 is thus rejected under 35 U.S.C. 103(a) as being unpatentable over Nakagawa together with Burghartz.

With respect to independent claim 24, Nakagawa discloses a p-channel metal-oxide-semiconductor transistor formed on a silicon substrate 12 (see the entire patent, particularly the Fig. 3 disclosure), comprising: a $Si_{1-x}Ge_x$ channel region 42, having a germanium molar fraction of x, and formed in the substrate, underneath a silicon dioxide (SiO_2) gate oxide "34" (note that Fig. 3's "34" is essentially a typo that should be "18," as per the Figs. 1-2 disclosure, and see column 4, lines 27-28) and between a source region 14 and a drain region 16; wherein x is less than equal to 0.6 (see column 3, lines 21-25), and wherein the $Si_{1-x}Ge_x$ channel region 42 forms a continuous $Si_{1-x}Ge_x$ / SiO_2 gate oxide interface (with SiO_2 gate oxide "34").

Nakagawa discloses that the SiO_2 gate oxide 18 of at least its Fig. 1 and Fig. 2 embodiments is "thermal silicon oxide" (see column 2, lines 49-56, for example), which means that it is formed by thermally oxidizing an underlying silicon layer (Fig. 1's silicon layer 20 and Fig. 2's silicon layer 34).

Nakagawa's Fig. 3 gate oxide "34" (again, such should be "18," as per the Figs. 1-2 disclosure) is apparently similarly formed by thermally oxidizing Fig. 3's $Si_{1-x}Ge_x$ channel region 42 (see column 5, lines 19-35). Nakagawa does not disclose that germanium oxide is present at Fig. 3's $Si_{1-x}Ge_x$ / SiO_2 gate oxide interface, but the applicant maintains: "germanium oxide will necessarily be created at [Nakagawa's] $Si_{1-x}Ge_x$ / SiO_2 gate oxide interface" (applicant's October 14, 2003 response at page 8, first paragraph). The applicant's argument is accepted in order to advance prosecution.

The apparent difference between claim 24 and Nakagawa, therefore, is claim 24 recites: "no germanium oxide is present at the $Si_{1-x}Ge_x$ / SiO_2 gate oxide interface."

Burghartz teaches forming a SiO_2 gate oxide on a SiGe channel layer by depositing a SiO_2 gate oxide layer on the SiGe layer instead of by thermally oxidizing the SiGe layer (see the entire patent, particularly the Fig. 3 disclosure).

It would have been obvious to one skilled in this art to form Nakagawa's Fig. 3 SiO_2 gate oxide "34" (again, such should be "18") by depositing a SiO_2 gate oxide layer on SiGe region 42 instead of by thermal oxidizing SiGe region 42, as per Burghartz's teaching (and such would result in there being no germanium oxide present at the $Si_{1-x}Ge_x$ / SiO_2 gate oxide interface because the SiGe region is not oxidized).

Claim 24 is thus rejected under 35 U.S.C. 103(a) as being unpatentable over Nakagawa together with Burghartz.

With respect to dependent claims 26 and 27, although Nakagawa is silent as to the thickness of its $Si_{1-x}Ge_x$ channel region 42, Burghartz also teaches that a SiGe channel region is typically 10-50 nm (100-500 angstroms) thick (see col. 7, lines 64-66).

It would have been further obvious to one skilled in this art to make Nakagawa's $Si_{1-x}Ge_x$ channel region 42 100-500 angstroms thick, because Burghartz teaches that $Si_{1-x}Ge_x$ channel regions are conventionally formed that thick.

Claims 26 and 27, at least insofar as understood, are thus rejected under 35 U.S.C. 103(a) as being unpatentable over Nakagawa together with Burghartz.

With respect to independent claim 28, Nakagawa discloses a p-channel metal-oxide-semiconductor transistor formed on a silicon substrate 12 (see the entire patent, particularly the Fig. 3 disclosure), comprising: a $Si_{1-x}Ge_x$ channel region 42, having a germanium molar fraction of 0.2 (see column 3, lines 21-25), and formed in the substrate, underneath a silicon dioxide (SiO_2) gate oxide "34" (note that Fig. 3's "34" is essentially a typo that should be "18," as per the Figs. 1-2 disclosure, and see column 4, lines 27-28) and between a source region 14 and a drain region 16, wherein the $Si_{1-x}Ge_x$ channel region 42 forms a continuous $Si_{1-x}Ge_x$ / SiO_2 gate oxide interface (with SiO_2 gate oxide "34").

Nakagawa discloses that the SiO_2 gate oxide 18 of at least its Fig. 1 and Fig. 2 embodiments is "thermal silicon oxide" (see column 2, lines 49-56, for example), which means that it is formed by thermally oxidizing an underlying silicon layer (Fig. 1's silicon layer 20 and Fig. 2's silicon layer 34).

Nakagawa's Fig. 3 gate oxide "34" (again, such should be "18," as per the Figs. 1-2 disclosure) is apparently similarly formed by thermally oxidizing Fig. 3's $Si_{1-x}Ge_x$

channel region 42 (see column 5, lines 19-35). Nakagawa does not disclose that germanium oxide is present at Fig. 3's $Si_{1-x}Ge_x$ / SiO_2 gate oxide interface, but the applicant maintains: "germanium oxide will necessarily be created at [Nakagawa's] $Si_{1-x}Ge_x$ / SiO_2 gate oxide interface" (applicant's October 14, 2003 response at page 8, first paragraph). The applicant's argument is accepted in order to advance prosecution.

The apparent difference between claim 28 and Nakagawa, therefore, is claim 28 recites: "no germanium oxide is present at the $Si_{1-x}Ge_x$ / SiO_2 gate oxide interface."

Burghartz teaches forming a SiO_2 gate oxide on a SiGe channel layer by depositing a SiO_2 gate oxide layer on the SiGe layer instead of by thermally oxidizing the SiGe layer (see the entire patent, particularly the Fig. 3 disclosure).

It would have been obvious to one skilled in this art to form Nakagawa's Fig. 3 SiO_2 gate oxide "34" (again, such should be "18") by depositing a SiO_2 gate oxide layer on SiGe region 42 instead of by thermal oxidizing SiGe region 42, as per Burghartz's teaching (and such would result in there being no germanium oxide present at the $Si_{1-x}Ge_x$ / SiO_2 gate oxide interface because the SiGe region is not oxidized).

Claim 28 is thus rejected under 35 U.S.C. 103(a) as being unpatentable over Nakagawa together with Burghartz.

With respect to independent claim 38, Nakagawa discloses a semiconductor transistor (see the entire patent, including the Fig. 3 disclosure), comprising: a silicon substrate 12; a silicon dioxide (SiO_2) gate oxide, coupled to the substrate; a gate 22, coupled to the SiO_2 gate oxide; source/drain regions 14 and 16 formed in the substrate on opposite sides of the gate; and a $Si_{1-x}Ge_x$ channel region 42, having a germanium molar fraction of x, and located underneath the SiO_2 gate oxide and between the

source/drain regions, wherein x is less than or equal to 0.6 (see column 3, lines 21-25), and wherein the $Si_{1-x}Ge_x$ channel region forms a continuous $Si_{1-x}Ge_x$ / SiO_2 gate oxide interface (with SiO_2 gate oxide "34").

Nakagawa discloses that the SiO_2 gate oxide 18 of at least its Fig. 1 and Fig. 2 embodiments is "thermal silicon oxide" (see column 2, lines 49-56, for example), which means that it is formed by thermally oxidizing an underlying silicon layer (Fig. 1's silicon layer 20 and Fig. 2's silicon layer 34).

Nakagawa's Fig. 3 gate oxide "34" (again, such should be "18," as per the Figs. 1-2 disclosure) is apparently similarly formed by thermally oxidizing Fig. 3's $Si_{1-x}Ge_x$ channel region 42 (see column 5, lines 19-35). Nakagawa does not disclose that germanium oxide is present at Fig. 3's $Si_{1-x}Ge_x$ / SiO_2 gate oxide interface, but the applicant maintains: "germanium oxide will necessarily be created at [Nakagawa's] $Si_{1-x}Ge_x$ / SiO_2 gate oxide interface" (applicant's October 14, 2003 response at page 8, first paragraph). The applicant's argument is accepted in order to advance prosecution.

The apparent difference between claim 38 and Nakagawa, therefore, is claim 38 recites: "no germanium oxide is present at the $Si_{1-x}Ge_x$ / SiO_2 gate oxide interface."

Burghartz teaches forming a SiO_2 gate oxide on a SiGe channel layer by depositing a SiO_2 gate oxide layer on the SiGe layer instead of by thermally oxidizing the SiGe layer (see the entire patent, particularly the Fig. 3 disclosure).

It would have been obvious to one skilled in this art to form Nakagawa's Fig. 3 SiO_2 gate oxide "34" (again, such should be "18") by depositing a SiO_2 gate oxide layer on SiGe region 42 instead of by thermal oxidizing SiGe region 42, as per Burghartz's

teaching (and such would result in there being no germanium oxide present at the $Si_{1-x}Ge_x$ / SiO_2 gate oxide interface because the SiGe region is not oxidized).

Claim 38 is thus rejected under 35 U.S.C. 103(a) as being unpatentable over Nakagawa together with Burghartz.

With respect to dependent claim 39, although Nakagawa is silent as to the thickness of its $Si_{1-x}Ge_x$ channel region 42, Burghartz also teaches that a SiGe channel region is typically 10-50 nm (100-500 angstroms) thick (see column 7, lines 64-66).

It would have been further obvious to one skilled in this art to make Nakagawa's $Si_{1-x}Ge_x$ channel region 42 100-500 angstroms thick, because Burghartz teaches that $Si_{1-x}Ge_x$ channel regions are conventionally formed that thick.

Claim 39 is thus rejected under 35 U.S.C. 103(a) as being unpatentable over Nakagawa together with Burghartz.

With respect to independent claim 40, Nakagawa discloses a semiconductor transistor formed on a silicon substrate 12 (see the entire patent, particularly the Fig. 3 disclosure), comprising: a $Si_{1-x}Ge_x$ channel region 42, having a germanium molar fraction of 0.2 (see column 3, lines 21-25) formed in the substrate, underneath a silicon dioxide (SiO_2) gate oxide "34" (note that Fig. 3's "34" is essentially a typo that should be "18," as per the Figs. 1-2 disclosure, and see column 4, lines 27-28) and between a source region 14 and a drain region 16, wherein the $Si_{1-x}Ge_x$ channel region 42 forms a continuous $Si_{1-x}Ge_x$ / SiO_2 gate oxide interface (with SiO_2 gate oxide "34").

Nakagawa discloses that the SiO_2 gate oxide 18 of at least its Fig. 1 and Fig. 2 embodiments is "thermal silicon oxide" (see column 2, lines 49-56, for example), which

means that it is formed by thermally oxidizing an underlying silicon layer (Fig. 1's silicon layer 20 and Fig. 2's silicon layer 34).

Nakagawa's Fig. 3 gate oxide "34" (again, such should be "18," as per the Figs. 1-2 disclosure) is apparently similarly formed by thermally oxidizing Fig. 3's $Si_{1-x}Ge_x$ channel region 42 (see column 5, lines 19-35). Nakagawa does not disclose that germanium oxide is present at Fig. 3's $Si_{1-x}Ge_x$ / SiO_2 gate oxide interface, but the applicant maintains: "germanium oxide will necessarily be created at [Nakagawa's] $Si_{1-x}Ge_x$ / SiO_2 gate oxide interface" (applicant's October 14, 2003 response at page 8, first paragraph). The applicant's argument is accepted in order to advance prosecution.

The apparent difference between claim 40 and Nakagawa, therefore, is claim 40 recites: "no germanium oxide is present at the $Si_{1-x}Ge_x$ / SiO_2 gate oxide interface."

Burghartz teaches forming a SiO_2 gate oxide on a SiGe channel layer by depositing a SiO_2 gate oxide layer on the SiGe layer instead of by thermally oxidizing the SiGe layer (see the entire patent, particularly the Fig. 3 disclosure).

It would have been obvious to one skilled in this art to form Nakagawa's Fig. 3 SiO_2 gate oxide "34" (again, such should be "18") by depositing a SiO_2 gate oxide layer on SiGe region 42 instead of by thermal oxidizing SiGe region 42, as per Burghartz's teaching (and such would result in there being no germanium oxide present at the $Si_{1-x}Ge_x$ / SiO_2 gate oxide interface because the SiGe region is not oxidized).

Claim 40 is thus rejected under 35 U.S.C. 103(a) as being unpatentable over Nakagawa together with Burghartz.

Claim 32 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 25 and 41-43 are allowable over the prior art of record.

The prior art of record does not disclose or suggest the allowable semiconductor transistors taken as a whole, particularly as formed.

The applicant's arguments are moot in view of the new grounds of rejection.

Sameshima et al. (newly cited United States Patent 5,889,292) is relevant to this application.

Registered practitioners can telephone the examiner at (571) 272-1843. Any voicemail message left for the examiner must include the name and registration number of the registered practitioner calling, and the Application/Control (Serial) Number. Technology Center 2800's general telephone number is (571) 272-2800.

Mark Prenty

Mark V. Prenty
Primary Examiner